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APPLICANTS Hideyuki Matsuoka, Hoya, JAPAN; Satoru Yamada, Ome, JAPAN; Isamu Asano, Iruma, JAPAN; Ryo Nagai, Mizuho, JAPAN; Tomonori Sekiguchi, Kokubunji, JAPAN; Riichiro Takemura, Tokyo, JAPAN;				
** CONTINUING DATA ***** This application is a DIV of 09/592,648 06/13/2000 PAT 6,621,110				
** FOREIGN APPLICATIONS ***** JAPAN 11-166320 06/14/1999				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/27/2003				
Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Allowance Verified and Acknowledged _____ Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 19	TOTAL CLAIMS 6
				INDEPENDENT CLAIMS 1
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TITLE SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A METHOD OF MANUFACTURE THEREOF				
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